

# **APPENDIX G**

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**US 9,843,786**

# US 9,843,786



(12) **United States Patent**  
**Shepherd**

(10) **Patent No.:** US 9,843,786 B2  
(45) **Date of Patent:** \*Dec. 12, 2017

- Title: Transport of stereoscopic image data over a display interface

(54) **TRANSPORT OF STEREOSCOPIC IMAGE DATA OVER A DISPLAY INTERFACE**

(71) **Applicant:** KONINKLIJKE PHILIPS N.V., Eindhoven (NL)

(72) **Inventor:** Nicoll Burleigh Shepherd, Coulsdon (GB)

(73) **Assignee:** KONINKLIJKE PHILIPS N.V., Eindhoven (NL)

(\*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) **Appl. No.:** 15/256,839

(22) **Filed:** Sep. 6, 2016

(65) **Prior Publication Data**

US 2016/0373720 A1 Dec. 22, 2016

**Related U.S. Application Data**

(63) Continuation of application No. 14/629,642, filed on Feb. 24, 2015, now Pat. No. 9,462,258, which is a (Continued)

(30) **Foreign Application Priority Data**

Dec. 18, 2007 (EP) ..... 07123461

(51) **Int. CL**  
*H04N 5/60* (2006.01)  
*H04N 13/00* (2006.01)

(Continued)

(52) **U.S. Cl.**  
CPC ..... *H04N 13/0059* (2013.01); *H04N 5/067* (2013.01); *H04N 5/60* (2013.01); (Continued)

(58) **Field of Classification Search**  
CPC ..... H04N 13/0402; H04N 5/60; H04N 5/067 (Continued)

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

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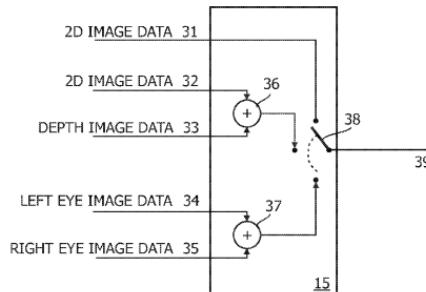
JP H0530538 A 2/1993  
JP 2003111101 A 4/2003 (Continued)

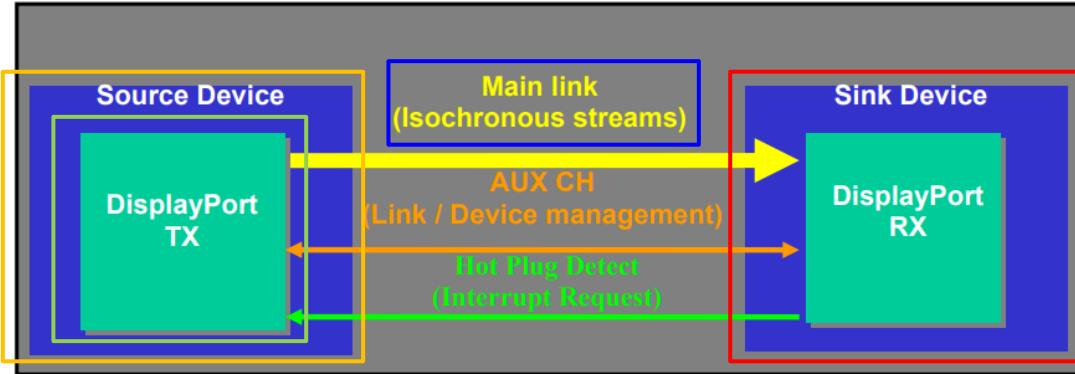
**Primary Examiner** — Nam Pham

(57) **ABSTRACT**

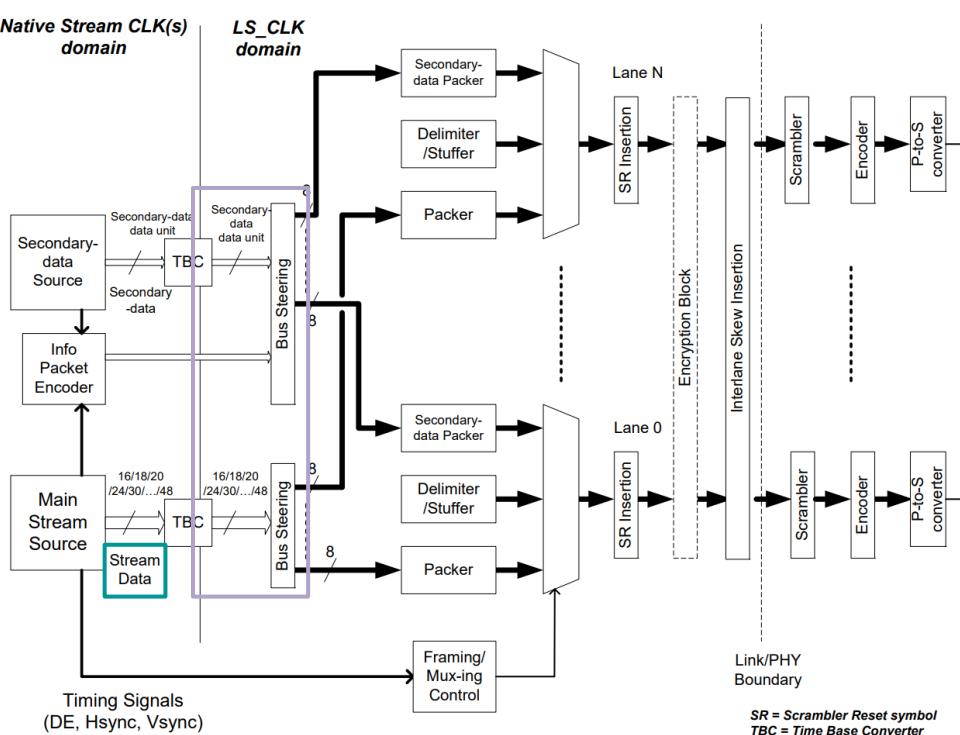
A digital display interface (40) connects a first audio-visual device (10) to a second audio-visual device (20). Stereoscopic image data is transmitted over the display interface (40). Components of stereoscopic image data are multiplexed and inserted into an image data carrying element. An existing deep color mode can be re-used for this purpose. Signaling information to help identify or decode the stereoscopic image data is carried in auxiliary data carrying elements. Stereoscopic image data can be distributed between image data carrying data elements and auxiliary data carrying data elements. Auxiliary data carrying elements can be transmitted in horizontal or vertical blanking periods, and can comprise HDMI Data Island Packets. Stereoscopic image data can be sent over an auxiliary data channel. The auxiliary data channel can form part of the same cable as is used to carry a primary channel of the display interface, a separate cable, or a wireless link.

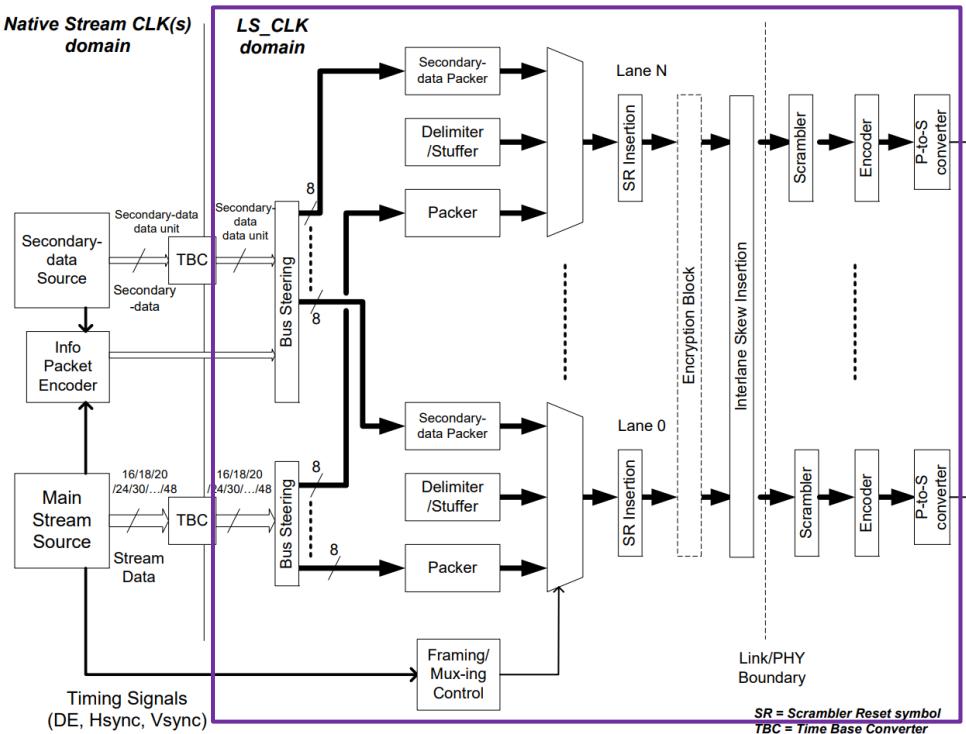
**22 Claims, 3 Drawing Sheets**



Claim 1	VESA DisplayPort Standard v1.2
<p>1. An interface part for a digital display, for use in a first audio-visual device for supporting a digital display transmission interface between the first audio-visual device and a second audio-visual device, the interface for transmitting uncompressed pixel information, the interface part comprising:</p>	<p><b>1.7 Overview of DisplayPort</b> A DisplayPort link consists of a main link, an auxiliary channel (AUX CH), and a Hot Plug Detect (HPD) signal line.</p> <p><b>As shown in Figure 2-45: DisplayPort Data Transport Channels</b></p> <p>below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used to transport isochronous data streams such as uncompressed video and audio. The auxiliary channel is a half-duplex bidirectional channel used for link management and device control. The HPD signal also serves as an interrupt request by the Sink device. In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-Legacy converter.</p>  <p><b>Figure 1-1: DisplayPort Data Transport Channels</b></p>

Claim 1	VESA DisplayPort Standard v1.2
<p>1. An interface part for a digital display, for use in a first audio-visual device for supporting a digital display transmission interface between the first audio-visual device and a second audio-visual device, <a href="#">the interface for transmitting uncompressed pixel information</a>, the interface part comprising:</p>	<p><b>1.7 Overview of DisplayPort</b></p> <p>A DisplayPort link consists of a main link, an auxiliary channel (AUX CH), and a Hot Plug Detect (HPD) signal line.</p> <p><b>As shown in Figure 2-45: DisplayPort Data Transport Channels</b></p> <p>below, the Main Link is a unidirectional, high-bandwidth and low-latency channel used below, <a href="#">the Main Link</a> is a unidirectional, high-bandwidth and low-latency channel used to <a href="#">transport isochronous data streams such as uncompressed video and audio</a>. The auxiliary channel is a half-duplex bidirectional channel used for link management and device control. The HPD signal also serves as an interrupt request by the Sink device.</p> <p>In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-Legacy converter.</p>

Claim 1	VESA DisplayPort Standard v1.2
<p>an input for receiving image data;</p>	<p><b>2.2.1 Main Stream to Main Link Lane Mapping in the Source Device</b></p> <p>The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with secondary-data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for transport over the main link. <u>The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.</u></p>  <p><b>Native Stream CLK(s) domain</b></p> <p><b>LS_CLK domain</b></p> <p><b>Link/PHY Boundary</b></p> <p><b>Timing Signals (DE, Hsync, Vsync)</b></p> <p><b>SR = Scrambler Reset symbol</b>  <b>TBC = Time Base Converter</b></p> <p><b>Figure 2-8: High Level Block Diagram of DP uPacket TX Main Link Data Path</b></p>

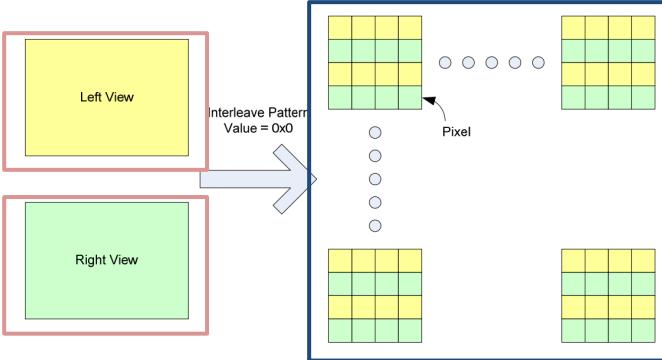
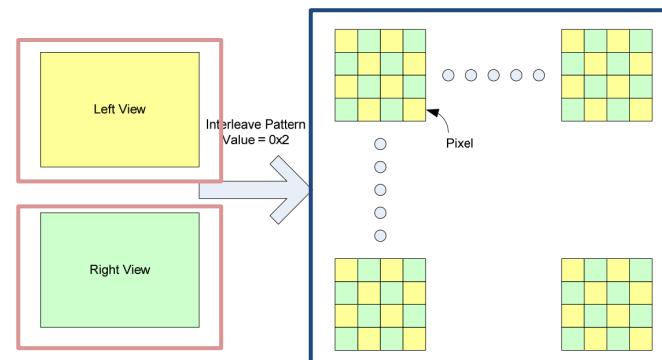
Claim 1	VESA DisplayPort Standard v1.2
<p>a formatter configured to format the received digital data for <u>transport over a transmission interface</u>, wherein the formatter is operable in:</p>	<p><b>2.2.1 Main Stream to Main Link Lane Mapping in the Source Device</b></p> <p>The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with secondary-data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for <u>transport over the main link</u>. The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.</p>  <p><b>Native Stream CLK(s) domain</b></p> <p><b>LS_CLK domain</b></p> <p><b>Link/PHY Boundary</b></p> <p><b>SR = Scrambler Reset symbol</b> <b>TBC = Time Base Converter</b></p> <p><b>Figure 2-8: High Level Block Diagram of DP uPacket TX Main Link Data Path</b></p>

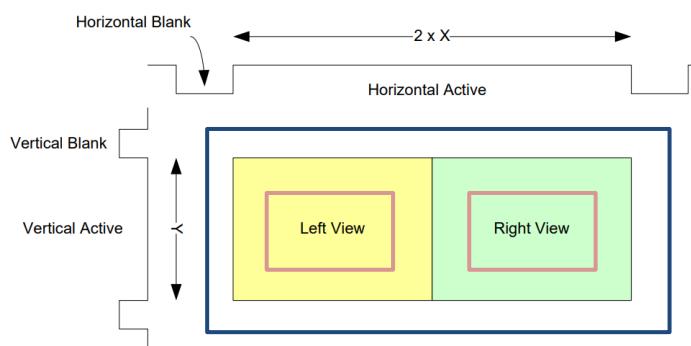
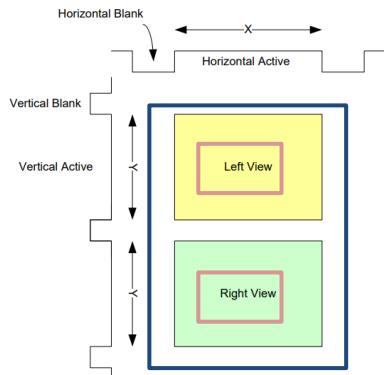
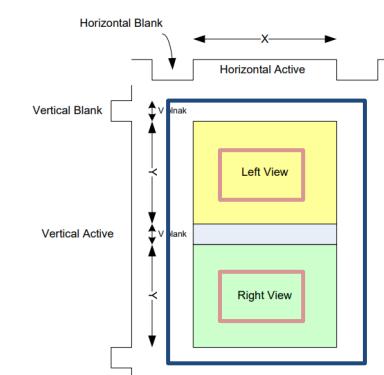
Claim 1	VESA DisplayPort Standard v1.2
<p>a formatter configured to format the received digital data for <a href="#">transport over a transmission interface</a>, wherein the formatter is operable in:</p>	<h2>2 Link Layer</h2> <h3>2.1 SST Mode Introduction</h3> <p>This section describes the services provided by the link layer of DisplayPort in SST (single stream transport) mode. (Those sub-sections in this section that are applicable to both SST and MST modes are explicitly noted in the sub-section titles.) These services are:</p> <ul style="list-style-type: none"> <li>• Isochronous transport services over the main link</li> </ul> <p>The isochronous transport services, based on a micro-packet architecture, maps the video and audio streams onto the Main Link symbols with a set of rules, (explained in Section 2.2), so that the streams can be correctly re-constructed into the original format and time base in the Sink device.</p> <p>Figure 2-1: Overview of Link Layer Services</p>

US 9,843,786

Claim 1	VESA DisplayPort Standard v1.2				
<p>a first mode in which the formatter generates a stream of first data elements comprising pixel data of a 2D image; and;</p>	<p><b>2.2.1 Main Stream to Main Link Lane Mapping in the Source Device</b>  The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed with secondary-data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for transport over the main link. The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.</p> <p><b>2.2.4 Main Stream Attribute Data Transport</b>  This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as follows:</p> <ul style="list-style-type: none"> <li>• Miscellaneous1 (MISC1, 8 bits) <ul style="list-style-type: none"> <li>○ Stereo video attribute (bits 2:1) <ul style="list-style-type: none"> <li>▪ <u>00</u> = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using an SDP called Video_Stream_Configuration (VSC) Packet</li> </ul> </li> </ul> </li> </ul> <p><b>2.2.5.6 Video_Stream_Configuration (VSC) Packet</b>  A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.</p> <p><b>2.2.5.6.2 VSC Packet Payload</b>  Table below shows the bit definitions of VSC Packet payload</p> <p style="text-align: center;"><b>Table 2-56: VSC Packet Payload</b></p> <table border="1"> <thead> <tr> <th data-bbox="568 1157 1159 1244">DB0 bits 3:0 = Stereo Interface Method Code</th><th data-bbox="1159 1157 1762 1244">DB0 bits 7:4 = Stereo Interface Method-Specific Parameter</th></tr> </thead> <tbody> <tr> <td data-bbox="568 1244 1159 1268">0 = Non Stereo Video</td><td data-bbox="1159 1244 1762 1268">Must be set to 0x0</td></tr> </tbody> </table>	DB0 bits 3:0 = Stereo Interface Method Code	DB0 bits 7:4 = Stereo Interface Method-Specific Parameter	0 = Non Stereo Video	Must be set to 0x0
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Claim 1	VESA DisplayPort Standard v1.2								
<p><b>a second mode</b>, different from the first mode, <b>operating at different times than the first mode</b>, in which the formatter <b>generates a stream of second data elements</b> comprising a multiplexed combination of <b>components of a stereoscopic image</b>;</p>	<p>Comments: The phrase “operating at different times than the first mode” means that the second mode and the first mode cannot be operated at the same time.</p> <p><b>2.2.1 Main Stream to Main Link Lane Mapping in the Source Device</b>  The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). <b>Main stream data (the uncompressed video stream) must be packed, stuffed, framed</b> and, optionally, multiplexed with secondary-data and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping for transport over the main link. The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.</p> <p><b>2.2.5.6 Video_Stream_Configuration (VSC) Packet</b>  A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.</p> <p><b>Table 2-56: VSC Packet Payload</b></p> <table border="1" data-bbox="679 731 1576 1323"> <thead> <tr> <th data-bbox="679 731 1128 789">DB0 bits 3:0 = Stereo Interface Method Code</th><th data-bbox="1128 731 1576 789">DB0 bits 7:4 = Stereo Interface Method-Specific Parameter</th></tr> </thead> <tbody> <tr> <td data-bbox="679 789 1128 1105">0 = Non Stereo Video 1 = Frame/Field Sequential (Figure 6, illustrates the composed frame format as transmitted by the source)</td><td data-bbox="1128 789 1576 1105"> <p>Must be set to 0x0</p> <p><b>Frame/Field Sequential Type:</b></p> <p><b>Value 0x0:</b> Left &amp; Right view indication based on the MISC1 bit 2:1</p> <p><b>Value 0x1:</b> Right when Stereo Signal = 1</p> <p><b>Value 0x2:</b> Left when Stereo Signal = 1</p> <p>All other values for this field (0x3-0xF) are RESERVED for future use.</p> </td></tr> <tr> <td data-bbox="679 1105 1128 1264">2 = Stacked Frame (Figure 7, illustrates the composed frame format as transmitted by the source)</td><td data-bbox="1128 1105 1576 1264"> <p><b>Stacked Frame Type:</b></p> <p><b>Value 0x0:</b> Left view is on top and right view on bottom</p> <p>All other values for this field (0x1-0xF) are RESERVED for future use.</p> </td></tr> <tr> <td data-bbox="679 1264 1128 1323">3 = Pixel Interleaved</td><td data-bbox="1128 1264 1576 1323"> <p><b>Interleave Pattern Type:</b></p> <p>For interleave pattern type 1 through 4, a 2x2 pattern</p> </td></tr> </tbody> </table>	DB0 bits 3:0 = Stereo Interface Method Code	DB0 bits 7:4 = Stereo Interface Method-Specific Parameter	0 = Non Stereo Video 1 = Frame/Field Sequential (Figure 6, illustrates the composed frame format as transmitted by the source)	<p>Must be set to 0x0</p> <p><b>Frame/Field Sequential Type:</b></p> <p><b>Value 0x0:</b> Left &amp; Right view indication based on the MISC1 bit 2:1</p> <p><b>Value 0x1:</b> Right when Stereo Signal = 1</p> <p><b>Value 0x2:</b> Left when Stereo Signal = 1</p> <p>All other values for this field (0x3-0xF) are RESERVED for future use.</p>	2 = Stacked Frame (Figure 7, illustrates the composed frame format as transmitted by the source)	<p><b>Stacked Frame Type:</b></p> <p><b>Value 0x0:</b> Left view is on top and right view on bottom</p> <p>All other values for this field (0x1-0xF) are RESERVED for future use.</p>	3 = Pixel Interleaved	<p><b>Interleave Pattern Type:</b></p> <p>For interleave pattern type 1 through 4, a 2x2 pattern</p>
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<p>a second mode, different from the first mode, operating at different times than the first mode, in which the formatter generates a stream of second data elements comprising a multiplexed combination of components of a stereoscopic image;</p>	<p><b>2.2.5.6 Video_Stream_Configuration (VSC) Packet</b>  A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.</p>  <p><b>Figure 2-31: Interleave Pattern Corresponding to a Checkerboard Pattern with Alternating Left and Right Image Pixels</b></p>  <p><b>Figure 2-32: Field Sequential Stereo Format with Left View and Right View Indicated via MISC1 bits 2:1 Field of the MSA</b></p>  <p><b>Figure 2-33: Stacked Top, Bottom Stereo Format with Left View on Top and Right View on Bottom 2:1 Field of the MSA</b></p>

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<p>wherein the interface part is configured to send <a href="#">signaling information across the transmission interface</a>, the signaling information identifying which mode the formatter is using;</p>	<p><b>2.2.1 Main Stream to Main Link Lane Mapping in the Source Device</b>  The Main Link must have one, two, or four lanes, with each lane capable of transporting eight bits of data per link symbol clock (LS_Clk). Main stream data (the uncompressed video stream) must be packed, stuffed, framed and, optionally, multiplexed <u>with secondary-data</u> and inter-lane skewed before it is handed over to the PHY layer after the Link Layer data mapping <u>for transport over the main link</u>. The stream data must enter the link layer at the original stream clock (Strm_Clk) rate and must be delivered to the PHY layer at the LS_Clk rate after this mapping.</p> <p><b>2.2.5.6 <u>Video Stream Configuration (VSC) Packet</u></b>  A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.</p> <p><b>2.2.5.6.1 VSC Packet Header</b>  Table 2-55 describes the packet header bytes of VSC Packet</p> <p style="text-align: center;"><b>Table 2-55: Header Bytes of VSC Packet</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">Byte#</th><th style="text-align: center; padding: 2px;">Content</th></tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">HB0</td><td style="text-align: center; padding: 2px;"><u>Secondary-data Packet ID = 0</u></td></tr> <tr> <td style="text-align: center; padding: 2px;">HB1</td><td style="text-align: center; padding: 2px;">07h</td></tr> <tr> <td style="text-align: center; padding: 2px;">HB2</td><td style="text-align: center; padding: 2px;">Bits 4:0 = Revision Number = 01h Bits 7:5 = RESERVED (all 0s)</td></tr> <tr> <td style="text-align: center; padding: 2px;">HB3</td><td style="text-align: center; padding: 2px;">Bits 4:0 = Number of valid data bytes = 01h Bits 7:5 = RESERVED (all 0s)</td></tr> </tbody> </table>	Byte#	Content	HB0	<u>Secondary-data Packet ID = 0</u>	HB1	07h	HB2	Bits 4:0 = Revision Number = 01h Bits 7:5 = RESERVED (all 0s)	HB3	Bits 4:0 = Number of valid data bytes = 01h Bits 7:5 = RESERVED (all 0s)
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<p>wherein the signaling information comprises information with respect to a multiplexing scheme used in a second mode for enabling the second audio-visual device to determine a decoding scheme to be used to decode a stereoscopic image format being used in the second mode;</p>	<p><b>2.2.4 Main Stream Attribute Data Transport</b>  This section describes the Main Stream attribute data that are transported for the reproduction of the main video stream by the Sink. The attribute data is sent once per frame during the vertical blanking period of the main video stream. Those attributes must be as follows:</p> <ul style="list-style-type: none"> <li>• Miscellaneous1 (MISC1, 8 bits) <ul style="list-style-type: none"> <li>◦ Stereo video attribute (bits 2:1) <ul style="list-style-type: none"> <li>▪ <u>00</u> = No 3D stereo video in-band signaling done using this field, indicating either no 3D stereo video transported or the in-band signaling done using an SDP called <u>Video Stream Configuration (VSC) Packet</u></li> </ul> </li> </ul> </li> </ul> <p><b>2.2.5.6 Video Stream Configuration (VSC) Packet</b>  A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.</p> <p style="text-align: center;"><b>Table 2-56: VSC Packet Payload</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 2px;">DB0 bits 3:0 = Stereo Interface Method Code</th> <th style="text-align: center; padding: 2px;">DB0 bits 7:4 = Stereo Interface Method-Specific Parameter</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">0 = Non Stereo Video</td> <td style="text-align: center; padding: 2px;">Must be set to 0x0</td> </tr> <tr> <td style="text-align: center; padding: 2px;">1 = Frame/Field Sequential (Figure 6, illustrates the compositored frame format as transmitted by the source)</td> <td style="text-align: center; padding: 2px;"> <b>Frame/Field Sequential Type:</b>    <b>Value 0x0:</b>  Left &amp; Right view indication based on the MISC1 bit 2:1    <b>Value 0x1:</b>  Right when Stereo Signal = 1    <b>Value 0x2:</b>  Left when Stereo Signal = 1    All other values for this field (0x3-0xF) are RESERVED for future use. </td> </tr> <tr> <td style="text-align: center; padding: 2px;">2 = Stacked Frame (Figure 7, illustrates the compositored frame format as transmitted by the source)</td> <td style="text-align: center; padding: 2px;"> <b>Stacked Frame Type:</b>    <b>Value 0x0:</b>  Left view is on top and right view on bottom    All other values for this field (0x1-0xF) are RESERVED for future use. </td> </tr> <tr> <td style="text-align: center; padding: 2px;">3 = Pixel Interleaved</td> <td style="text-align: center; padding: 2px;"> <b>Interleave Pattern Type:</b>    For interleave pattern type 1 through 4, a 2x2 pattern </td> </tr> </tbody> </table>	DB0 bits 3:0 = Stereo Interface Method Code	DB0 bits 7:4 = Stereo Interface Method-Specific Parameter	0 = Non Stereo Video	Must be set to 0x0	1 = Frame/Field Sequential (Figure 6, illustrates the compositored frame format as transmitted by the source)	<b>Frame/Field Sequential Type:</b>  <b>Value 0x0:</b> Left & Right view indication based on the MISC1 bit 2:1  <b>Value 0x1:</b> Right when Stereo Signal = 1  <b>Value 0x2:</b> Left when Stereo Signal = 1  All other values for this field (0x3-0xF) are RESERVED for future use.	2 = Stacked Frame (Figure 7, illustrates the compositored frame format as transmitted by the source)	<b>Stacked Frame Type:</b>  <b>Value 0x0:</b> Left view is on top and right view on bottom  All other values for this field (0x1-0xF) are RESERVED for future use.	3 = Pixel Interleaved	<b>Interleave Pattern Type:</b>  For interleave pattern type 1 through 4, a 2x2 pattern
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Claim 1	VESA DisplayPort Standard v1.2																														
<p>wherein the signaling information comprises information with respect to a multiplexing scheme used in a second mode for enabling the second audio-visual device to determine a decoding scheme to be used to decode a stereoscopic image format being used in the second mode;</p>	<p>grid (as shown in figure 2) is used to illustrate the interleaving pattern of the composited stereo frame.</p> <p><b>Value 0x0:</b> Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on even lines. The corresponding 2x2 pattern is shown below:</p> <table border="1" data-bbox="864 439 1084 568"> <tr> <td>Composited Frame's 1<sup>st</sup> Active Line</td> <td>Left View Pixel</td> <td>Left View Pixel</td> </tr> <tr> <td>Composited Frame's 2<sup>nd</sup> Active Line</td> <td>Right View Pixel</td> <td>Right View Pixel</td> </tr> </table> <p><b>Value 0x1:</b> Interleave pattern corresponding to 2-way horizontally interleaved stereo where right view pixels are on odd lines. The corresponding 2x2 pattern is shown below:</p> <table border="1" data-bbox="864 684 1084 813"> <tr> <td>Composited Frame's 1<sup>st</sup> Active Line</td> <td>Right View Pixel</td> <td>Right View Pixel</td> </tr> <tr> <td>Composited Frame's 2<sup>nd</sup> Active Line</td> <td>Left View Pixel</td> <td>Left View Pixel</td> </tr> </table> <p><b>Value 0x2:</b> Interleave pattern corresponding to a checkerboard pattern with alternating left and right view pixels starting with left view pixel. The corresponding 2x2 pattern is shown below:</p> <table border="1" data-bbox="864 957 1084 1087"> <tr> <td>Composited Frame's 1<sup>st</sup> Active Line</td> <td>Left View Pixel</td> <td>Right View Pixel</td> </tr> <tr> <td>Composited Frame's 2<sup>nd</sup> Active Line</td> <td>Right View Pixel</td> <td>Left View Pixel</td> </tr> </table> <p><b>Value 0x3:</b> Interleave pattern corresponding to 2-way vertically interleaved stereo starting with left view pixels. The corresponding 2x2 pattern is shown below:</p> <table border="1" data-bbox="1632 295 1785 424"> <tr> <td>Composited Frame's 1<sup>st</sup> Active Line</td> <td>Left View Pixel</td> <td>Right View Pixel</td> </tr> <tr> <td>Composited Frame's 2<sup>nd</sup> Active Line</td> <td>Left View Pixel</td> <td>Right View Pixel</td> </tr> </table> <p><b>Value 0x4:</b> Interleave pattern corresponding to 2-way vertically interleaved stereo starting with right view pixels. The corresponding 2x2 pattern is shown below:</p> <table border="1" data-bbox="1632 554 1785 684"> <tr> <td>Composited Frame's 1<sup>st</sup> Active Line</td> <td>Right View Pixel</td> <td>Left View Pixel</td> </tr> <tr> <td>Composited Frame's 2<sup>nd</sup> Active Line</td> <td>Right View Pixel</td> <td>Left View Pixel</td> </tr> </table> <p>All other values for this field (0x5-0xF) are RESERVED for future use.</p> <p><b>Value 0x0:</b> A value of 0x0 indicate left half of the image represents left EYE view and right half represents right EYE view</p> <p><b>Value 0x1:</b> A value of 0x1 indicate left half of the image represents right EYE view and right half represents left EYE view</p> <p>All other values for this field (0x2-0xF) are RESERVED for future use.</p> <p>Values 0x5-0xF are RESERVED</p>	Composited Frame's 1 <sup>st</sup> Active Line	Left View Pixel	Left View Pixel	Composited Frame's 2 <sup>nd</sup> Active Line	Right View Pixel	Right View Pixel	Composited Frame's 1 <sup>st</sup> Active Line	Right View Pixel	Right View Pixel	Composited Frame's 2 <sup>nd</sup> Active Line	Left View Pixel	Left View Pixel	Composited Frame's 1 <sup>st</sup> Active Line	Left View Pixel	Right View Pixel	Composited Frame's 2 <sup>nd</sup> Active Line	Right View Pixel	Left View Pixel	Composited Frame's 1 <sup>st</sup> Active Line	Left View Pixel	Right View Pixel	Composited Frame's 2 <sup>nd</sup> Active Line	Left View Pixel	Right View Pixel	Composited Frame's 1 <sup>st</sup> Active Line	Right View Pixel	Left View Pixel	Composited Frame's 2 <sup>nd</sup> Active Line	Right View Pixel	Left View Pixel
Composited Frame's 1 <sup>st</sup> Active Line	Left View Pixel	Left View Pixel																													
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Claim 1	VESA DisplayPort Standard v1.2
wherein <u>the signaling information</u> comprises <u>information with respect to a multiplexing scheme used in a second mode</u> for enabling the second audio-visual device to determine a decoding scheme to be used to decode a stereoscopic image format being used in the second mode;	<p><b>13 Appendix H: Protocol Support for 3D Stereo Display</b></p> <p>With 10.8Gbps over 4 lanes, DisplayPort provides sufficient bandwidth for transporting up to 1080p (FHD) 3D Stereo video data at 120Hz (that is, 60Hz each for left and right frames). At 21.6Gbps over 4 lanes, the bandwidth is enough for 1080p 3D Stereo video at 240Hz (that is, 120Hz each for left and right frames).</p> <p><b>13.1 In-band 3D Stereo Signaling Methods</b></p> <p>In addition, the DisplayPort standard provides for two in-band mechanisms through which a Source device can specify the attribute of the 3D stereo video format it is transmitting. One method uses an MSA MISC1 field and the other method uses a Secondary-Data Packet called VSC Packet.</p> <p>A Sink device with DPCD Revision 1.2 or higher must support both methods.</p>

Claim 1	VESA DisplayPort Standard v1.2
<p>wherein the formatter is configured to generate a <b>stream of data elements</b> comprising either the first or second data elements and <b>auxiliary data</b> carrying data elements at <b>intervals</b> in the stream; and</p>	<p><b>2.2.1.3 Main Video Stream Data Packing</b> The link layer must first steer pixel data in a pixel-within-lane manner as shown in Table 2-2.</p> <ul style="list-style-type: none"><li>• <u>SS (Secondary-data Start)</u><ul style="list-style-type: none"><li>○ Inserted at the beginning of secondary-data</li></ul></li><li>• <u>SE (Secondary-data End)</u><ul style="list-style-type: none"><li>○ Inserted at the end of the secondary-data</li></ul></li></ul> <p><b>2.2.1.5 Main Stream Attribute/Secondary-Data Packet Insertion</b> The dummy stuffing data symbols during the video blanking periods (both vertical and horizontal) may be substituted either with main stream attributes data or a <u>secondary-data packet</u>. Both must be framed with <u>SS</u> and <u>SE</u> control symbols as shown in Figure 2-14.</p>

## Claim 1

wherein the formatter is configured to generate a **stream of data elements** comprising either the first or second data elements and **auxiliary data** carrying data elements at **intervals** in the stream; and

## VESA DisplayPort Standard v1.2

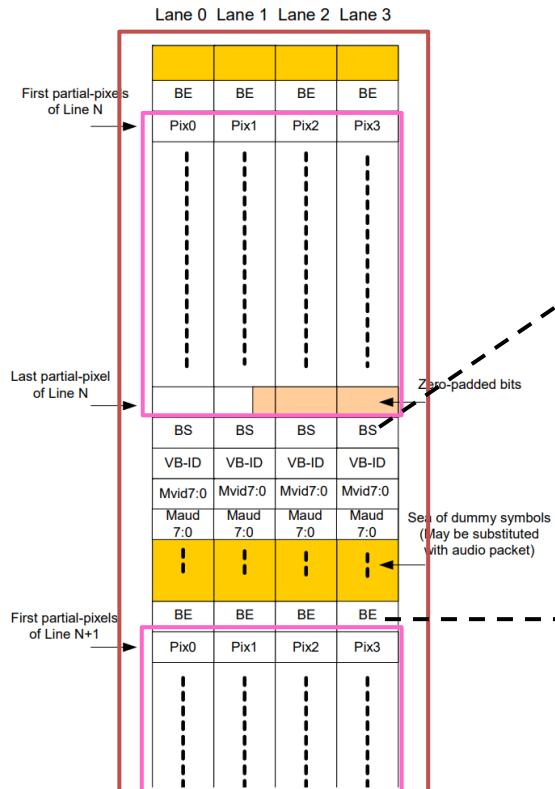


Figure 2-10: Main Video Stream Data Packing Example for a Four Lane Main Link

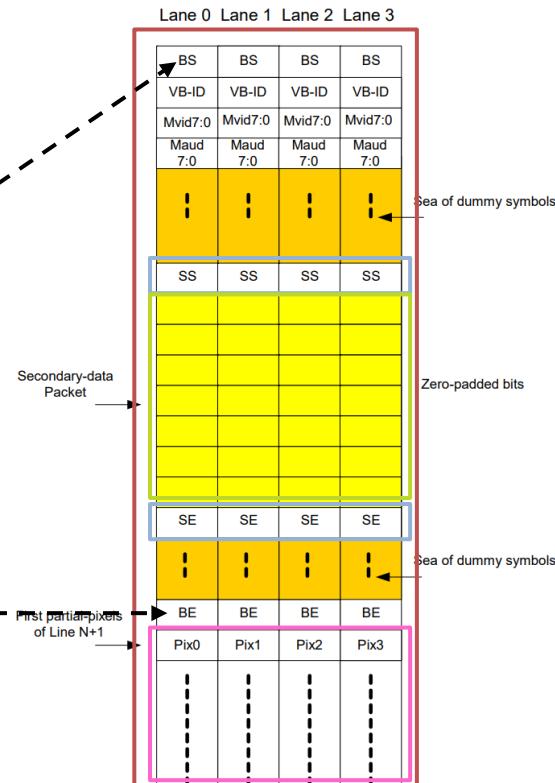


Figure 2-14: Secondary-Data Insertion

Claim 1	VESA DisplayPort Standard v1.2																				
<p>the signaling information being carried in the auxiliary data elements.</p>	<p><b>2.2.5 Secondary-data Packing Formats</b>  Table 2-46 shows how the secondary-data packet is constructed.</p> <p><b>Table 2-46: Secondary-data Packet Header</b></p> <table border="1"> <thead> <tr> <th data-bbox="591 364 860 429">Byte#</th><th data-bbox="860 364 1781 429">Content</th></tr> </thead> <tbody> <tr> <td data-bbox="591 429 860 462">HB0</td><td data-bbox="860 429 1781 462">Secondary-data Packet ID</td></tr> <tr> <td data-bbox="591 462 860 495">HB1</td><td data-bbox="860 462 1781 495">Secondary-data Packet type</td></tr> <tr> <td data-bbox="591 495 860 528">HB2</td><td data-bbox="860 495 1781 528">Secondary-data-packet-specific header byte0</td></tr> <tr> <td data-bbox="591 528 860 561">HB3</td><td data-bbox="860 528 1781 561">Secondary-data-packet-specific header byte1</td></tr> </tbody> </table> <p><b>2.2.5.6 Video Stream Configuration (VSC) Packet</b>  A DP Source device may send 3D Stereo in-band signaling using VSC Packet by setting MSA Packet MISC1 field bits 2:1 to 00.</p> <p><b>2.2.5.6.1 VSC Packet Header</b>  Table 2-55 describes the packet header bytes of VSC Packet</p> <p><b>Table 2-55: Header Bytes of VSC Packet</b></p> <table border="1"> <thead> <tr> <th data-bbox="591 868 744 933">Byte#</th><th data-bbox="744 868 1781 933">Content</th></tr> </thead> <tbody> <tr> <td data-bbox="591 933 744 966">HB0</td><td data-bbox="744 933 1781 966">Secondary-data Packet ID = 0</td></tr> <tr> <td data-bbox="591 966 744 999">HB1</td><td data-bbox="744 966 1781 999">07h</td></tr> <tr> <td data-bbox="591 999 744 1077">HB2</td><td data-bbox="744 999 1781 1077">Bits 4:0 = Revision Number = 01h Bits 7:5 = RESERVED (all 0s)</td></tr> <tr> <td data-bbox="591 1077 744 1140">HB3</td><td data-bbox="744 1077 1781 1140">Bits 4:0 = Number of valid data bytes = 01h Bits 7:5 = RESERVED (all 0s)</td></tr> </tbody> </table>	Byte#	Content	HB0	Secondary-data Packet ID	HB1	Secondary-data Packet type	HB2	Secondary-data-packet-specific header byte0	HB3	Secondary-data-packet-specific header byte1	Byte#	Content	HB0	Secondary-data Packet ID = 0	HB1	07h	HB2	Bits 4:0 = Revision Number = 01h Bits 7:5 = RESERVED (all 0s)	HB3	Bits 4:0 = Number of valid data bytes = 01h Bits 7:5 = RESERVED (all 0s)
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